

Comments on a Character Recognition Method of Bledsoe and Browning*

A method of Bledsoe and Browning¹ for character recognition was tested at the Bell Telephone Laboratories, using the Generalized Scanner² as an input transducer and the IBM 704 to simulate the recognition logic. The recognition of both hand block printing and machine printing was studied.

The hand-printed data consisted of 50 alphabets of 36 characters, each alphabet printed by a different person. The printing was somewhat constrained by requiring these people to print on one-quarter-inch quad-ruled paper and asking them to print neatly and at a size approximating the ruled boxes on the paper. Thus, a total of 1800 semiconstrained alpha-numeric characters were studied.

The source of the machine printing was an IBM 407 line printer. Recognition of 50 samples of each of the ten machine-printed numerals was attempted.

Recognition for this method was tried for randomly chosen ordered exclusive pairs using a 12×12 scanning matrix and five samples to construct the "memory matrix." Centering was done in the same manner as suggested by Bledsoe and Browning; that is, the input pattern was shifted to the upper left-hand corner of the matrix.

It was felt that any results obtained with their method would be meaningless unless they were compared with the results of another recognition method operating on the same data.

The recognition method to which the results of Bledsoe and Browning's method were compared involves the comparison of an unknown input pattern (the same 12×12 matrix is used in both methods) to a set of average characters. The average characters are described by a set of 12×12 matrices (one for each character) in which each element represents the probability of occurrence of a mark in that element for the character which it represents. For example, there is one average character for *A*, one for *B*, and so on. The comparison of the unknown input pattern to the average characters is performed by computing a set of cross-correlation values, and the maximum value is chosen as a criterion for identification. The input pattern is shifted in two dimensions with respect to the average characters to account for off-center characters.

In both methods, letters were compared only to letters and numbers to numbers. The results are shown in Table I. The results obtained by Bledsoe and Browning are taken from their paper, and the results using their method are for samples of each character which were not used to make up the list. The results for the correlation method are based on all 50 samples. In the case of hand printing, the samples recognized were the

same samples which were used to construct the average characters; in the case of machine printing, recognition was tried for a different set of 50 samples of each numeral from that used to construct the probability matrices.

TABLE I
PER CENT RECOGNITION FOR VARIOUS TRIALS

	Results Obtained by Bledsoe and Browning	Duplication of Method of Bledsoe and Browning	Results of Correlation Method
Hand printing	78.4	19.6	77.2
Machine printing	100.0	86.7	99.6

It is evident that this study does not verify the results of Bledsoe and Browning. For the case of hand printing, the differences may be ascribed to the fact that their input data were generated by only one person rather than by a representative population.

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Improved Arrangement of a Decimal Multiplier*

Dr. Phister described a decimal multiplier¹ in his book, "Logical Design of Digital Computers." The product of two decimal digits is formed by adding, in a three-input adder, the proper combination of the multiplicand multiples (*Y*), (*-Y*), and (*4Y*). The (*-Y*) multiple is formed by the 10's complement of the multiplicand. A table is presented on page 307 of the book mentioned above which lists a combination for each of the nine possible multiples to be added. There are several other variations to the table which Dr. Phister does not list. With a rearrangement of the 2*Y* and 3*Y* adder input combinations, a reduction of better than one-third in the number of diodes necessary to build the adder inputs can be easily accomplished in a binary coded decimal machine.

The rearranged table is as follows.

Desired Product	The Adder Inputs		
	<i>X</i> ₁	<i>X</i> ₂	<i>X</i> ₃
<i>Y</i>	0	<i>Y</i>	0
2 <i>Y</i>	0	<i>Y</i>	<i>Y</i>
3 <i>Y</i>	0	- <i>Y</i>	4 <i>Y</i>
4 <i>Y</i>	4 <i>Y</i>	0	0
5 <i>Y</i>	4 <i>Y</i>	<i>Y</i>	0
6 <i>Y</i>	4 <i>Y</i>	<i>Y</i>	<i>Y</i>
7 <i>Y</i>	4 <i>Y</i>	- <i>Y</i>	4 <i>Y</i>
8 <i>Y</i>	4 <i>Y</i>	0	4 <i>Y</i>
9 <i>Y</i>	4 <i>Y</i>	<i>Y</i>	4 <i>Y</i>

To realize the reduction in number of diodes necessary to build this multiplier, let

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¹ W. W. Bledsoe and I. Browning, "Pattern recognition and reading by machine," *Proc. EJCC*, pp. 225-232; December, 1959.

² W. H. Highleyman and L. A. Kamensky, "A generalized scanner for pattern- and character-recognition studies," *Proc. WJCC*, pp. 291-294; March, 1959.

¹ M. Phister, Jr., "Logical Design of Digital Computers," John Wiley and Sons, Inc., New York, N. Y., pp. 305-311; 1958.

us look at a simple example. Two 8-4-2-1 decimal coded digits are to be multiplied by the above table. The multiplicand is contained in a register and the multiplier in a register, $R_1R_2R_3R_4$. Multiplication shall be done in one bit time, hence in a parallel-by-digit mode. Whether operating in parallel or serially, the diode reduction is the same. This is true because the multiple combinations, which are a function of the multiplier digits, must be determined before the multiplication of the multiplicand commences. The new adder input equations are

$$X_1 = Z_4R_4 + Z_1R_3 \text{ (6 diodes),}$$

$$X_2 = Z_1R_1\bar{R}_2 + Z_1\bar{R}_1R_2 + Z_{-1}R_1R_2 \text{ (12 diodes),}$$

$$X_3 = Z_4R_4 + Z_1\bar{R}_1R_2 + Z_4R_1R_2 \text{ (11 diodes).}$$

In these equations, Z_4 means the output of the 4*Y* multiple generator, Z_1 means the multiplicand (*Y*) delayed in a serial machine, and Z_{-1} is the (*-Y*) multiple or the complemented multiplicand.

The number of diodes required to make up these adder input gates can be compared with the number required to make up the equations on page 311 of Phister's book. The author calculates that 44 diodes are necessary to construct the adder inputs of Dr. Phister's multiple combination scheme. Using the same gate construction rules, he calculates that only 29 diodes are necessary to construct the adder inputs of the multiple combination scheme described in this letter.

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Computation of an Expression for the Frequency Spectrum of a Two-Sided Signal*

For the purpose of this discussion we will define a two-sided signal, $s(t)$, to be one which is not identically zero and which is of class L_1 everywhere within the open interval $(-\infty, +\infty)$. The frequency spectrum, $S(\omega)$, of this signal is conventionally determined by taking the Fourier transform of $s(t)$ as:

$$S(\omega) = \int_{-\infty}^{+\infty} s(t)\epsilon^{-j\omega t} dt. \quad (1)$$

If $S(\omega)$ is determined by machine, then it is calculated for a large number of values of ω to yield finally a tabular form for $S(\omega)$. It is to be noted further that a machine calculation can, in general, carry out an integration in the variable t only over a finite interval, say $(-T, +T)$. Thus, the machine would,

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